



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/577,069

06/20/2006

Masahiko Hata

7372/88130

4111

42798 7590 04/01/2009
FITCH, EVEN, TABIN & FLANNERY
P. O. BOX 18415
WASHINGTON, DC 20036

EXAMINER

SLUTSKER, JULIA

ART UNIT

PAPER NUMBER

2891

MAIL DATE

DELIVERY MODE

04/01/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/577,069	Applicant(s) HATA ET AL.	
	Examiner JULIA SLUTSKER	Art Unit 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 December 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>translation of JP-H06-349731</u> . |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori'731 (JP 6-349731).

Regarding claim 1, Mori discloses epitaxially growing a compound semiconductor functional layer (Fig.4a, numerals 21, 32,6,3), on a substrate (Fig.4a, numeral 4); bonding a support substrate (Fig.4c, numeral 41) to the compound semiconductor layer (paragraph [0058]); polishing the substrate and a part of the compound functional semiconductor layer on the side which is in contact with the substrate, to remove them (Fig.4c; paragraph [0058]); bonding a thermally conductive substrate (Fig.4D, numeral 1, paragraph [0059]) having a thermal conductivity higher than that of substrate (4) (note: substrate (4) is InP, [0054], and substrate (1) is Si) to the exposed surface of the compound semiconductor functional layer (3) to obtain a multilayer substrate and separating the support substrate (41) from the multilayer substrate (Fig.4e, [0060]).

Regarding claim 2, Mori discloses that the compound semiconductor functions layer includes at least two layers (Fig.4a, 21, 32, 6, 3).

Regarding claim 3, Mori discloses that the compound semiconductor functional layer includes at least one selected form the group consisting of In, Ga and at least one selected form the group consisting of N and As [0054]).

Regarding claim 4, Mori discloses that the thermally conductive substrate includes Si ([0059])

3. Claims 5-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Sano (US 6, 916,676).

Regarding claim 5, Sano discloses a method for manufacturing a compound semiconductor substrate, comprising the steps of: epitaxially growing a compound semiconductor functional layer (column 19, lines 40-45; Fig.1a, numeral 2) on a substrate (Fig.1a, numeral 1), bonding a thermally conductive substrate (Fig.2a, numeral 11) having a thermal conductivity higher than that of the substrate (1) (note: (1) is sapphire, column 19, lines 42-45; (11) is AlN, column 24, lines 21-25); polishing the substrate (1) and a part on the compound semiconductor functional layer (2) on the side which is in contact with substrate (1) to remove them (Fig.2C, column 25, lines 14-20) .

Regarding claim 6, Sano discloses that the compound semiconductor functional layer (2) includes at least two layers (column 20, lines 24-30).

Regarding claim 7, Sano discloses that the compound semiconductor functional layer includes at least one selected from the group consisting of Ga and Al (column 20,

Art Unit: 2891

lines 25-30) and at least one selected from the group consisting of N(column 20, lines 50-53).

Regarding claim 8, Sano discloses that the thermally conductive substrate includes at least one selected from the group consisting of Al, Cu, Mo, W, diamond, SiC, AlN and Si (column 24, lines 23-26).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Mori.

Regarding claim 9, Mori discloses all limitations of claim 1 for reasons above.

Mori does not disclose a step of forming an electrode on the resultant compound semiconductor device. However, it would have been obvious to one of ordinary skill in the art at time the invention was made to form an electrode on the resultant compound semiconductor devices for the purpose of using this structure as a light emitting diode.

Response to Arguments

6. Applicant's arguments filed 12/29/2008 have been fully considered but they are not persuasive.

7. The applicant's arguments that Mori does not disclose "polishing the substrate (1) and a part of the functional layer (2) which is in contact with (1) to remove them" are not persuasive since Mori discloses polishing the substrate and a part of the compound

Art Unit: 2891

functional semiconductor layer on the side which is in contact with the substrate, to remove them (Fig.4c; paragraph [0058]))

8. The applicant's arguments that Mori does not disclose "bonding a thermally conductive substrate to the exposed surface of the functional layer" are not persuasive since Mori discloses bonding a thermally conductive substrate (Fig.4D, numeral 1, paragraph [0059]) having a thermal conductivity higher than that of substrate (4) (note: substrate (4) is InP, [0054], and substrate (1) is Si) to the exposed surface of the compound semiconductor functional layer (3).

9. The applicant's arguments that Sano does not disclose "polishing a part of the compound semiconductor functional layer (22) on the side that is in contact with the substrate (21) to remove them" are not persuasive since Sano discloses polishing the substrate (1) and a part on the compound semiconductor functional layer (2) on the side which is in contact with substrate (1) to remove them (Fig.2C, column 25, lines 14-20).

10. The applicant's arguments that the period for responding to the Office Action should be reset since Applicant's representatives do not have an English translation of Mori (JP 6-349731) are not persuasive, since the Office is not required to send the translation of foreign documents to the Applicant with a Non-Final Office action and the translation should be obtained prior to the appeal conference so that the participants the appeal conference can consider the translation (see MPEP 1207.02 [R-3]). Examiner also would like to point out that the document of Mori (JP 6-349731) has been cited in the IDS form and therefore the content of this document should be known to the

Art Unit: 2891

Applicant. Nevertheless, the machine translation of Mori (JP 6-349731) is sent with the present Office Action.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2891

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

March 23, 2009

/Asok K. Sarkar/

Primary Examiner, Art Unit 2891

March 28, 2009